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1 KDB: a multi-threaded debugger for multi-threaded applications

Peter A. Buhr, Martin Karsten, Jun Shih

January 1996 **Proceedings of the SIGMETRICS symposium on Parallel and distributed tools**

Full text available: pdf(991.10 KB) Additional Information: full citation, references, citings, index terms

2 Parasight: a high-level debugger/profiler architecture for shared-memory multiprocessor

Z. Aral, Ilya Gertner

June 1988 **Proceedings of the 2nd international conference on Supercomputing**

Full text available: pdf(764.60 KB) Additional Information: full citation, abstract, references, citings, index terms

Existing debuggers and profilers are inadequate for debugging and profiling parallel programs. They are awkward in their handling of multiple threads of control and highly intrusive in their monitoring of program behavior. ParasightTM is an architecture that is geared towards non-intrusive high-level debugging and profiling. Parasight controls and observes the execution of parallel programs in terms of the set of abstractions that are being employed by the programmer. D ...

3 Replay for concurrent non-deterministic shared-memory applications

Mark Russinovich, Bryce Cogswell

May 1996 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1996 conference on Programming language design and implementation**, Volume 31 Issue 5

Full text available: pdf(968.81 KB) Additional Information: full citation, abstract, references, citings, index terms

Replay of shared-memory program execution is desirable in many domains including cyclic debugging, fault tolerance and performance monitoring. Past approaches to repeatable execution have focused on the problem of re-executing the shared-memory access patterns in parallel programs. With the proliferation of operating system supported threads and shared memory for uniprocessor programs, there is a clear need for efficient replay of concurrent applications. The solutions for parallel systems can b ...

Keywords: instruction counter, non-determinism, repeatable execution, shared memory

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1 Advances in hardware/software co-simulation techniques: A timing-accurate HW/SW co-simulation of an ISS with SystemC

Luca Formaggio, Franco Fummi, Graziano Pravadelli

September 2004 **Proceedings of the 2nd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: pdf(243.62 KB) Additional Information: full citation, abstract, references, index terms

The paper presents a system level co-simulation methodology for modeling, validating, and analyzing the performance of embedded systems. The proposed solution relies on the integration between an instruction set simulator (ISS) and the SystemC simulation kernel. In this way, the ISS is used to abstract the model of the real programmable device where the SW should run, while SystemC is used to model HW components that interact with the SW. A correct validation of such an architecture is infeasibl ...

Keywords: co-simulation, system level modeling

2 A thread-aware debugger with an open interface

Daniel Schulz, Frank Mueller

August 2000 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 2000 ACM SIGSOFT international symposium on Software testing and analysis**, Volume 25 Issue 5

Full text available: pdf(347.13 KB) Additional Information: full citation, abstract, references, citings, index terms

While threads have become an accepted and standardized model for expressing concurrency and exploiting parallelism for the shared-memory model, debugging threads is still poorly supported. This paper identifies challenges in debugging threads and offers solutions to them. The contributions of this paper are threefold. First, an open interface for debugging as an extension to thread implementations is proposed. Second, extensions for thread-aware debugging are identified and implemented wit ...

Keywords: active debugging, concurrency, debugging, open interface, threads

3 Space-efficient scheduling of parallelism with synchronization variables

Guy E. Blelloch, Phillip B. Gibbons, Girija J. Narlikar, Yossi Matias

June 1997 **Proceedings of the ninth annual ACM symposium on Parallel algorithms and architectures**

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1. **Debugging aids for systems-on-a-chip**
Bannatyne, R.;
Northcon/98 Conference Proceedings
21-23 Oct. 1998 Page(s):159 - 163
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